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EXAMINER	
LEE, CHUN KUAN	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/806,787	SETHI ET AL.	
	Examiner	Art Unit	
	Chun-Kuan Lee	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 May 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,6,8-16 and 18-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,6,8-16 and 18-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/16/08 & 7/11/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

RESPONSE TO ARGUMENTS

1. Applicant's arguments filed 05/20/2008 have been fully considered but they are not persuasive. Rejection of claims 8, 11 and 17 under 35 U.S.C. 112 second paragraph is withdrawn. Currently, claims 3-5, 7, 17 and 21 are canceled, and claims 1-2, 6, 8-16 and 18-20 are pending for examination.

2. In response to applicant's arguments (on page 6, 2nd paragraph) regarding the amended independent claim 1 rejected under 35 U.S.C. 103(a) that the combination of references do not teach/suggest the amended claimed limitation "connected by a plurality of point to point links" and "an entire configuration space is globally visible to the first and second processor" because such claimed features are not taught/suggested by AAPA; applicant's arguments have fully been considered, but are not found to be persuasive.

The examiner respectfully disagrees, as the examiner relies on "BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors" for the teaching of the above claimed features as following:

connected by a plurality of point to point links (BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors, p. 21, p. 204 and HyperTransport™ Technology I/O Link, pp. 6-8; Fig. 2 on p. 8; Fig. 10 on p. 20; 'The HyperTransport™ Technology Solution' Section on p. 4); and

an entire configuration space is globally visible to the first and second processor (BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors, p. 21; p. 25 and HyperTransport™ Technology I/O Link, pp. 6-8; Fig. 2 on p. 8; pp. 15-16; Fig. 10 on p. 20), wherein the I/O streaming between the processors and the devices requires all the devices to be visible to the processors, thus enabling entire configuration space is globally visible to both processors.

As the applicant is applying the above arguments for the amended independent claim 1 towards amended independent claim 15, the examiner will also apply the above response to the amended independent claim 15.

3. In response to applicant's arguments (on page 6, last paragraph) regarding the amended independent claim 6 rejected under 35 U.S.C. 103(a) that the combination of references do not teach/suggest the amended claimed feature of retrieving a port number using a node identifier that itself is retrieved using a configuration address associated with an I/O configuration access because such claimed feature is not taught by Downer; applicant's arguments have fully been considered, but are not found to be persuasive.

Please note that one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Wherein the examiner relied in the references as following for the teaching of the above claimed feature:

BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors teaches retrieving a node identifier using a configuration address associated with an I/O configuration access (p. 21; Sec. 8.3 on p. 204 and HyperTransport™ Technology I/O Link, Chapter 7 on pp. 67-69; Chapter 9 on p. 109).

Downer teaches retrieving a port number (e.g. Port ID) using a node identifier (e.g. Node ID) (Fig. 1; col. 11, ll. 18-37 and col. 12, 25-54).

As the applicant is applying the above arguments for the amended independent claim 6 towards amended independent claims 12 and 18, the examiner will also apply the above response to the amended independent claims 12 and 18.

I. ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

4. As required by **M.P.E.P. 609(C)**, the applicant's submissions of the Information Disclosure Statement dated June 16, 2008 and July 11, 2008 are acknowledged by the examiner and the cited references have been considered in the examination of the claims now pending. As required by **M.P.E.P 609 C(2)**, a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

II. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 2 and 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in view of "BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors".

6. As per claim 1, AAPA teaches a method comprising:

converting (e.g. decoding) a configuration access corresponding to a memory address or Input Output (IO) address within a decoder of a second processor (Drawings, Processor 1 of Figure 1), the second processor coupled to a first processor (Drawings, Processor 2 of Figure 1), for configuration (Specification, page 2, ll. 16-24); and

the second processor (Drawings, Processor 1 of Figure 1) directly connected to the integrated device of the first processor (Drawings, Processor 2 of Figure 1).

AAPA does not teach the method comprising:

a configuration cycle for configuration of the integrated device in the first processor ...; and

routing the configuration cycle from the decoder to the first processor ... .

BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors teaches a method for configuring an integrated device in a first processor (e.g. processor node or application processor (AP)) (Sec. 2.1 on p. 21 and Sec. 2.1.4 on p. 23) comprising:

a configuration cycle for configuration of an integrated device in a first processor (e.g. AP), wherein the first processor is coupled (e.g. with the second processor) to a network fabrics comprising a plurality of point to point links (Sec. 2.1 on p. 21; Sec. 2.1.4 on p. 23; Sec. 3.1 on p. 25 and p. 204), as the system operates in accordance to Hyper Transport Technology, wherein the Hyper Transport Technology discloses the corresponding configuration cycle (HyperTransport™ Technology I/O Link, 'The HyperTransport™ Technology Solution' Sec. on page 4; Fig. 10 on p. 20; Chapter 7 on p. 67 and Chapter 9 on p. 109), wherein address range FD_FE00_0000h to FD_FFFF_FFFFh is associated with the configuration; and

routing the configuration cycle from a decoder (e.g. decoder in the BSP) to the first processor (e.g. AP) based at least in part on a routing information to configure the integrated device from an unconfigured state to a configured state, wherein an entire configuration space is globally visible to processors (e.g. first and second processors) (pp. 21-22; p. 25; Sec. 2.1.4 on p. 23; Sec. 3.1 on p. 25; Chapter 8 on p. 203 and HyperTransport™ Technology I/O Link, pp. 6-8; Fig. 2 on p. 8; pp. 15-16; Fig. 10 on p. 20), wherein the I/O streaming between the processors and the devices requires all the devices to be visible to the processors, thus enabling entire configuration space is globally visible to both processors.

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors' routing of configuration cycle into AAPA's multi-processor system for the benefit of enabling the proper configuration of the processors

via the utilization of Hyper Transport technology having high-speed, high-performance, point-to-point link for interconnection the processors to obtain the invention as specified in claim 1.

7. As per claim 2, AAPA and BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors teach all the limitations of claim 1 as discussed above, where BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors further teaches the method comprising wherein the configuration cycle is routed via the network fabric (BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors, p. 21, p. 204 and HyperTransport™ Technology I/O Link, Fig. 10 on p. 20; 'The HyperTransport™ Technology Solution' Sec. on p. 4).

8. As per claim 15, AAPA teaches a system comprising:

a first processor (Drawings, Processor 1 of Figure 1) with a decoder coupled to a second network component (Drawings, Processor 2 of Figure 1) with an integrated device, the decoder to decode either a memory or IO configuration access for configuration(Specification, page 2, ll. 14-24); and

the processor (Drawings, Processor 1 of Figure 1) directly connected to the integrated device of the second network component (Drawings, Processor 2 of Figure 1).

AAPA does not teach the system comprising:

a configuration cycle for configuration of the integrated device; and

to transmit the configuration cycle to the integrated device, wherein the configuration cycle adheres to a first type of interconnect protocol.

BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors teaches a system and a method comprising:

a configuration cycle for configuration of an integrated device of a second network component (e.g. AP) (Sec. 2.1 on p. 21; Sec. 2.1.4 on p. 23 and Sec. 3.1 on p. 25), as the system operates in accordance to Hyper Transport Technology, wherein the Hyper Transport Technology discloses the corresponding configuration cycle (HyperTransport™ Technology I/O Link, Chapter 7 on p. 67 and Chapter 9 on p. 109), wherein address range FD_FE00_0000h to FD_FFFF_FFFFh is associated with the configuration;

to transmit (e.g. transmit via routing) the configuration cycle to the integrated device, wherein the configuration cycle adheres to a first type of interconnect protocol (e.g. Hyper Transport link) and is routed to the integrated device via a network fabric comprising a plurality of point to point links, and wherein an entire configuration space is globally visible to a first processor and the second network component (pp. 21-22; Sec. 2.1.4 on p. 23; Sec. 3.1 on p. 25 and Chapter 8 on pp. 203-204 and HyperTransport™ Technology I/O Link, pp. 6-8; Fig. 2 on p. 8; pp. 15-16; Fig. 10 on p. 20; 'The HyperTransport™ Technology Solution' Sec. on p. 4), wherein the I/O streaming between the processors and the devices requires all the devices to be visible to the

processors, thus enabling entire configuration space is globally visible to both processors.

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors' routing of configuration cycle into AAPA's multi-processor system for the benefit of enabling the proper configuration of the processors via the utilization of Hyper Transport technology having high-speed, high-performance, point-to-point link for interconnection the processors to obtain the invention as specified in claim 15.

9. As per claim 16, AAPA and BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors teach all the limitations of claim 15 as discussed above, where BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors further teaches the system comprising wherein the first type of interconnection protocol comprises a PCI type protocol (BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors, pp. 21-22 and Sec. 3.1 on p. 25 and HyperTransport™ Technology I/O Link, Fig. 10 on p. 20).

10. Claims 6, 8-14 and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in view of "BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors" and Downer et al. (US Patent 6,910,108).

11. As per claim 6, AAPA teaches a method comprising:

decoding an Input Output (IO) configuration access within a second processor (Drawings, Processor 1 of Figure 1), coupled to a first processor (Drawings, Processor 2 of Figure 1), for configuration (Specification, page 2, ll. 16-24); and

the second processor (Drawings, Processor 1 of Figure 1) directly connected to the integrated device of a first processor (Drawings, Processor 2 of Figure 1).

AAPA does not teach the method comprising:

a configuration cycle for configuration of the integrated device in the first processor;

wherein the decoding includes retrieving a node identifier ...; and

routing the configuration cycle including the node identifier and the port number from the second processor ... .

BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors teaches a method for configuring an integrated device in a first processor (e.g. processor node or application processor (AP)) (Sec. 2.1 on p. 21 and Sec. 2.1.4 on p. 23) comprising:

a configuration cycle for configuration of an integrated device in a first processor (e.g. AP) (Sec. 2.1 on p. 21; Sec. 2.1.4 on p. 23 and Sec. 3.1 on p. 25), as the system operates in accordance to Hyper Transport Technology, wherein the Hyper Transport Technology discloses the corresponding configuration cycle (HyperTransport™

Technology I/O Link, Chapter 7 on p. 67 and Chapter 9 on p. 109), wherein address range FD_FE00_0000h to FD_FFFF_FFFFh is associated with the configuration; and

decoding (e.g. decoding via initialization) includes retrieving a node identifier (e.g. node ID) using a configuration address associated with the IO configuration access (p. 21; Sec. 8.3 on p. 204 and HyperTransport™ Technology I/O Link, Chapter 7 on pp. 67-69; Chapter 9 on p. 109); and

routing the configuration cycle including a transaction address (e.g. configuration address) and the node identifier (e.g. Node ID) from a second processor (e.g. BSP) to the integrated device in the first processor (e.g. AP) based at least in part on a routing information to configure the integrated device from an unconfigured state to a configured state (pp. 21-22; Sec. 2.1.4 on p. 23; pp. 25-26 and Chapter 8 on pp. 203-204), wherein the configuration address register including the configuration address is needed for specifying and routing to the target.

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors' routing of configuration cycle into AAPA's multi-processor system for the benefit of enabling the proper configuration of the processors via the utilization of Hyper Transport technology having high-speed, high-performance, point-to-point link for interconnection the processors to obtain the invention as specified in claim 6.

AAPA and BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors do not expressly teach the method comprising retrieving a port number using the node identifier.

Downer teaches a multiprocessor system and method comprising retrieving a port number (e.g. Port ID) using a node identifier (e.g. node ID) (Fig. 1; col. 11, ll. 18-37 and col. 12, 25-34), wherein the retrieving is implemented by utilizing a received address data.

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include Downer's Port ID into AAPA and BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors' decoding process for the benefit of increasing the accuracy and robustness in the routing of data to obtain the invention as specified in claim 6.

12. As per claim 8, AAPA, BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors and Downer teach all the limitations of claim 6 as discussed above, where BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors further teaches the method comprising wherein a network fabric that route the configuration cycle is a plurality of point to point links (BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors, p. 21, p. 204 and HyperTransport™ Technology I/O Link, Fig. 10 on p. 20; 'The HyperTransport™ Technology Solution' Sec. on p. 4).

13. As per claim 9, AAPA, BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors and Downer teach all the limitations of claim 6 as discussed above, where BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors further teaches the method comprising wherein the configuration adheres to an interconnection of predetermined protocol (e.g. PCI protocol) (BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors, pp. 21-22 and Sec. 3.1 on p. 25 and HyperTransport™ Technology I/O Link, Fig. 10 on p. 20).

14. As per claim 10, AAPA, BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors and Downer teach all the limitations of claim 9 as discussed above, where BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors further teaches the method comprising wherein the predetermined protocol comprises a PCI type interconnect protocol (BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors, pp. 21-22 and Sec. 3.1 on p. 25 and HyperTransport™ Technology I/O Link, Fig. 10 on p. 20).

15. As per claim 11, AAPA, BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors and Downer teach all the limitations of claim 8 as discussed above, where AAPA and BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors further teach the method comprising wherein the second processor is coupled to the first processor via a network fabric

(AAPA, Specification, p. 2, ll. 11-17; BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors, p. 21, p. 204 and HyperTransport™ Technology I/O Link, Fig. 10 on p. 20; 'The HyperTransport™ Technology Solution' Sec. on p. 4).

16. As per claim 12, AAPA teaches a processor (Drawings, Processor 1 of Figure 1) comprising:

a decoder to decode either a memory or IO configuration access for configuration (Specification, page 2, ll. 14-24);

the processor (Drawings, Processor 1 of Figure 1) directly connected to the integrated device of a second processor (Drawings, Processor 2 of Figure 1).

AAPA does not teach the processor comprising:

a configuration cycle for configuration of the integrated device of the second processor ... ; and

to transmit the configuration cycle to the integrated device.

BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors teaches a system and a method comprising:

processors are coupled by a plurality of point to point links (p. 21, p. 204 and HyperTransport™ Technology I/O Link, Fig. 10 on p. 20; 'The HyperTransport™ Technology Solution' Section on p. 4);

a configuration cycle for configuration of an integrated device of a second processor (e.g. AP) (Sec. 2.1 on p. 21; Sec. 2.1.4 on p. 23 and Sec. 3.1 on p. 25), as the system operates in accordance to Hyper Transport Technology, wherein the Hyper Transport Technology discloses the corresponding configuration cycle (HyperTransport™ Technology I/O Link, Chapter 7 on p. 67 and Chapter 9 on p. 109), wherein address range FD_FE00_0000h to FD_FFFF_FFFFh is associated with the configuration,

decoding (e.g. decoding via initialization) include receive a configuration address and provide a transaction address (e.g. configuration address), and a node identifier (e.g. node ID) corresponding to an address range of the configuration address (e.g. FD_FE00_0000h to FD_FFFF_FFFFh) (pp. 21-22; Sec. 2.1.4 on p. 23; pp. 25-26 and Chapter 8 on pp. 203-204 and HyperTransport™ Technology I/O Link, Chapter 7 on pp. 67-69; Chapter 9 on p. 109), wherein the configuration address register including the configuration address is needed for specifying and routing to the target; and

a range of node identifier (e.g. Node ID1, Node ID 2, etc) associated with the configuration cycle (pp. 21-22 and pp. 203-204)

to transmit (e.g. transmit via routing) the configuration cycle to the integrated device (pp. 21-22; Sec. 2.1.4 on p. 23; Sec. 3.1 on p. 25 and Chapter 8 on pp. 203-204).

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors' routing of configuration cycle into AAPA's multi-

processor system for the benefit of enabling the proper configuration of the processors via the utilization of Hyper Transport technology having high-speed, high-performance, point-to-point link for interconnection the processors to obtain the invention as specified in claim 12.

AAPA and BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors do not expressly teach the system comprising providing a port identifier corresponding to the node identifier.

Downer teaches a multiprocessor system and method comprising providing a port identifier (e.g. Port ID) corresponding to the node identifier (e.g. node ID) (Fig. 1; col. 11, ll. 18-37 and col. 12, 25-54).

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include Downer's Port ID into AAPA and BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors' decoding process for the benefit of increasing the accuracy and robustness in the routing of data to obtain the invention as specified in claim 12.

17. As per claim 13, AAPA, BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors and Downer teach all the limitations of claim 12 as discussed above, where BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors further teaches the processor comprising wherein the transmission of the configuration to either the chip set or integrated device is via a PCI

type interconnection (BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors, pp. 21-22 and Sec. 3.1 on p. 25 and HyperTransport™ Technology I/O Link, Fig. 10 on p. 20).

18. As per claim 14, AAPA, BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors and Downer teach all the limitations of claim 12 as discussed above, where BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors further teaches the processor comprising wherein the configuration cycle is to be routed to the integrated device via a network fabric (BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors, p. 21, p. 204 and HyperTransport™ Technology I/O Link, Fig. 10 on p. 20; 'The HyperTransport™ Technology Solution' Sec. on p. 4).

19. As per claim 18, AAPA teaches an article of manufacture comprising:

a machine-readable storage medium having stored thereon a plurality of machine readable instructions, wherein when the instructions are executed by a system (Drawings, Figure 1 and Specification, page 2, ll. 9-24), the instructions provide for configuration comprising:

decoding either a memory or IO configuration access to a configuration cycle in a decoder of a second processor (Drawings, Processor 1 of Figure 1) for configuration (Specification, page 2, ll. 14-24); and

the second processor (Drawings, Processor 1 of Figure 1) directly connected an integrated device the processor (Drawings, Processor 2 of Figure 1).

AAAP does not teach the article comprising:

a configuration cycle for configuring the integrated device in the processor;

wherein the decoder is to receive a configuration address ... ;

transmitting the configuration cycle from the second processor ... .

BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors teaches a system and a method comprising:

a configuration cycle for configuration of an integrated device of a processor (e.g. AP) (Sec. 2.1 on p. 21; Sec. 2.1.4 on p. 23 and Sec. 3.1 on p. 25), as the system operates in accordance to Hyper Transport Technology, wherein the Hyper Transport Technology discloses the corresponding configuration cycle (HyperTransport™ Technology I/O Link, Chapter 7 on p. 67 and Chapter 9 on p. 109), wherein address range FD_FE00_0000h to FD_FFFF_FFFFh is associated with the configuration,

decoding (e.g. decoding via initialization) include receive a configuration address and provide a transaction address (e.g. configuration address), and a node identifier (e.g. node ID) corresponding to an address range of the configuration address with the configuration cycle (e.g. FD_FE00_0000h to FD_FFFF_FFFFh) (pp. 21-22; Section 2.1.4 on p. 23; pp. 25-26 and Chapter 8 on pp. 203-204 and HyperTransport™ Technology I/O Link, Chapter 7 on pp. 67-69; Chapter 9 on p. 109), wherein the

configuration address register including the configuration address is needed for specifying and routing to the target; and

a range of node identifier (e.g. Node ID1, Node ID 2, etc) associated with the configuration cycle (pp. 21-22 and pp. 203-204)

transmitting (e.g. transmit via routing) the configuration cycle from a second processor (e.g. BSP) to the integrated device, wherein the configuration cycle adheres to a first type of interconnect protocol (e.g. Hyper Transport link); (pp. 21-22; Sec. 2.1.4 on p. 23; Sec. 3.1 on p. 25 and Chapter 8 on pp. 203-204).

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors' routing of configuration cycle into AAPA's multi-processor system for the benefit of enabling the proper configuration of the processors via the utilization of Hyper Transport technology having high-speed, high-performance, point-to-point link for interconnection the processors to obtain the invention as specified in claim 18.

AAPA and BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors do not expressly teach the system comprising providing a port identifier corresponding to the node identifier.

Downer teaches a multiprocessor system and method comprising providing a port identifier (e.g. Port ID) corresponding to a node identifier (e.g. node ID) (Fig. 1; col. 11, ll. 18-37 and col. 12, 25-54).

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include Downer's Port ID into AAPA and BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors' decoding process for the benefit of increasing the accuracy and robustness in the routing of data to obtain the invention as specified in claim 18.

20. As per claim 19, AAPA, BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors and Downer teach all the limitations of claim 18 as discussed above, where BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors further teaches the article of manufacture comprising wherein the integrated device is coupled to the decoder of the second processor coupled to the processor or network component via a network fabric (BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors, p. 21, p. 204 and HyperTransport™ Technology I/O Link, Fig. 10 on p. 20; 'The HyperTransport™ Technology Solution' Sec. on p. 4).

21. As per claim 20, AAPA, BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors and Downer teach all the limitations of claim 18 as discussed above, where BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors further teaches the article of manufacture comprising wherein the first type of interconnect protocol is in accordance with a PCI type protocol (BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™

Processors, pp. 21-22 and Sec. 3.1 on p. 25 and HyperTransport™ Technology I/O Link, Fig. 10 on p. 20).

III. CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

b. DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

IMPORTANT NOTE

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/C.K.L./

August 15, 2008

Chun-Kuan (Mike) Lee
Examiner
Art Unit 2181

/Alford W. Kindred/

Supervisory Patent Examiner, Art Unit 2181